

DIGITAL FILTER

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Abstract

PURPOSE: To reduce a coefficient revision time considerably without increase in the scale by providing a data generator comprising an adder, a delay circuit and a coefficient register to each tap in the digital filter employing a RAM for the multiplication.

CONSTITUTION: Data generators 10a to 10d or the like of the same configuration are provided to taps of the digital filter and data information from an input terminal 1 and coefficient information from the generators 10a to 10d are multiplied by corresponding RAMs 5a to 5d and filtered information is outputted from an output terminal 3. A coefficient signal from a coefficient data input terminal 2 is stored in a register 11 based on a control signal from control input terminals 4A, 4B and accumulated by a delay circuit 14 and an adder circuit 15 to provide an output of the coefficient information and the coefficient is revised in parallel in each tap thereby reducing the coefficient calculation time considerably. As a result, the processing time is 896 clocks (=265+64) in the case of an 8-bit input for 640 tap provision, and then the small sized and high speed filter is realized.

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